REMARKS

This is intended as a full and complete response to the Office Action dated September 10, 2007, having a shortened statutory period for response set to expire on December 10, 2007. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-42 are pending in the application. Claims 1-42 remain pending following entry of this response.

Claim Rejections - 35 U.S.C. § 103

Claims 1-42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dean et al. (6,604,174).

Applicant respectfully traverses this rejection.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the first criteria.

The Federal Circuit has held that even if all of the elements of a claimed invention are found in a combination of prior art references, analysis requires "consideration of two factors:

(1) whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process; and

(2) whether the prior art would also have revealed that in so making or carrying out, those of ordinary skill would have a reasonable expectation of success."

PharmaStem Therapeutics, Inc. v. ViaCell, Inc., 491 F.3d 1342 (Fed. Cir. 2007)

In this regard the Federal Circuit points out that in *KSR International Co. vs. Teleflex, Inc.*, 127 S. Ct. 1727 (2007) the Supreme Court "acknowledged the importance of identifying 'a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does' in an obviousness determination." *Takeda Chemical Industries, Ltd. v. Alphaphram Pty, Ltd.*, 492 F.3d 1350, 1356 (Fed. Cir. 2007).

KSR suggests that in some cases, the fact that something is "obvious to try" may be sufficient to make it obvious under 103. However, the Federal Circuit has pointed out that there is a prohibition against the "obvious to try" rationale in two situations, i.e., (1) "one must be motivated to do more than merely to 'vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no indication as to which of many possible choices is likely to succeed,' " and (2) "[s]imilarly, prior art fails to provide the requisite 'reasonable expectation' of success where it teaches merely to pursue a 'general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it.' " *Medichem, S.A. v. Rolabo*, S.L., 437 F.3d 1157, 1165, 77 USPQ2d 1865, 1870 (Fed. Cir. 2006), quoting *In re O'Farrell*, 853 F.2d 894, 903 (Fed. Cir. 1988), 7 USPQ2d 1673, 1681.

In this case, the Examiner fails to provide sufficient reasoning for modifying the reference teachings to yield the elements as claimed. Specifically, the Examiner states:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Dean to implement the private cache architecture (also disclosed by Dean) since the groups of cache ways disclosed by Dean already act as independent caches and independent caches also contain cache ways. Therefore, the cache way allocation techniques of the invention could be well implemented in a private cache system. (*Office Action*, p.3)

Applicant respectfully submits that the Examiner's explanation is merely a statement that *Dean* "could be" modified in the manner suggested. Thus, the Examiner fails to articulate any particular reasons for why the reference should be modified in precisely the way suggested by the Examiner to yield the claimed invention. "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness". *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); cited with approval in *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1740-41 (2007).

Applicant further submits that, while *Dean* mentions private cache architectures, it does not teach or suggest that the allocation techniques of *Dean* should be modified to fit private cache architectures. The portion of *Dean* that mentions private cache architectures states:

> Currently, there are two primary architectures for multiple processors. The first is for each processor to have a local cache; the second is for a secondary cache between the processors and the main memory. The latter type of cache is referred to as a "unified" cache. With a unified cache, a processor requesting data queries the secondary cache over a common memory bus after gaining control of that bus.
>
> This scheme has several drawbacks. First, the main memory bus is shared between the processors, meaning that only a single request can be honored at a time. Also, multiple cache look ups can create a bottleneck. The individual processor may not be able to handle several lines of information at a time. Moreover, the amount of cache space set aside for each processor in these systems is usually fixed.
>
> Thus, the most prevalent unified caches allow only single requests, can have cache access bottlenecks, and have fixed cache space per processor. What is needed is a system that solves these problems. *Dean*, column 2, lines 46-63.

The above material is included in the Background section of *Dean*, and describes "two primary architectures for multiple processors," one architecture of local caches for each

processor, and a second architecture of a unified cache. The description of the unified cache architecture is followed by a description of the drawbacks of the unified cache architecture, and the statement "[w]hat is needed is a system that solves these problems." Clearly, the above passage establishes that, of the two possible architectures, *Dean* is solely directed to solving the drawbacks of the unified cache architecture. That is, *Dean* does not teach that the included allocation techniques should be modified to fit private cache architectures. Rather, after mentioning private caches, *Dean* proceeds to narrow the focus of the invention to unified cache architectures. Thus, *Dean* in fact teaches away from the modification proposed by the Examiner.

For the above reasons, Applicant submits that the Examiner has not provided a *prima facie* case of obviousness as required by MPEP § 2143. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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